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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,375	08/18/2003	Chien-Ping Huang	59744 (71987)	4812

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EXAMINER
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OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/643,375

Applicant(s)

HUANG ET AL.

Examiner

Douglas W. Owens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 9-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2 and 5 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,701,614 to Ding et al.

Regarding claim 1, Ding et al. teach a semiconductor package (Fig. 4h) having bumps on a chip comprising:

at least one chip (30) having an active surface (31) and an opposite inactive surface (32), and having a plurality of bond pads (34) on the active surface;

a plurality of conductive bumps (51) formed on the bond pads of the chip;

an encapsulation body (40, 61) for encapsulating the chip and the conductive bumps, wherein ends of the conductive bumps are exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

a plurality of first conductive traces (72) formed on the encapsulation body and electrically connected to the exposed ends of the conductive bumps;

a solder mask (91) applied over the first conductive traces and having a plurality of openings for exposing predetermined portions of first conductive traces; and

a plurality of solder balls (92; Col. 5, lines 24 – 28) formed on exposed portions of the first conductive traces.

Regarding claim 2, Ding et al. teach a semiconductor device, further comprising:  
at least one dielectric layer (81) and a plurality of second conductive traces ((72); wherein, conductive traces 71 are taken as the first conductive traces) formed on the dielectric layer;

the dielectric layer and the second conductive traces interposed between the first conductive traces (71) and the solder mask layer (91);

wherein the dielectric layer is located on the first conductive traces and has a plurality of vias by which the predetermined portions of the first conductive traces are exposed and electrically connected to the second conductive traces, and the solder mask is located on the second conductive traces whose predetermined portions are exposed via the openings for the solder mask layer and respectively connected to the plurality of solder balls.

Regarding claims 5 and 6, Ding et al. teach a semiconductor package, wherein the conductive bump is a solder bump (Col. 4, lines 8 – 16).

Regarding claims 7, Ding et al. teach a semiconductor package, wherein the exposed portions of the first conductive traces are terminals.

Regarding claims 8, Ding et al. teach a semiconductor package, wherein the exposed portions of the second conductive traces are terminals.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al. as applied to claims 1 and 2 above, and further in view of US Patent No. 6,734,534 to Vu et al.

Ding et al. do not teach a semiconductor package, wherein the inactive surface of the chip is exposed outside of the encapsulation body. Vu et al. teach a semiconductor package (Fig. 15), wherein the inactive surface (118) of the chip (114) is exposed outside of the encapsulation body (102). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Vu et al. into the device taught by Ding et al., since it is desirable to provide smaller packages for use in mobile systems, such as handheld devices (See Vu et al., Col. 3, lines 18 – 24).

***Response to Arguments***

5. Applicant's arguments filed December 16, 2004 have been fully considered but they are not persuasive.

Applicant argues that Ding et al. do not teach a semiconductor package including an encapsulation body for encapsulating a chip and a plurality of conductive bumps. This teaching can be seen in Fig. 4h, where encapsulating material 40 encapsulates the

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chip on the bottom and side portions, and the dielectric layer 61 disposed over the chip and conductive bumps completes the encapsulation of the chip and plurality of conductive bumps. The two dielectric bodies combine to form a complete encapsulation body.

Applicant argues that Ding et al. do not teach a semiconductor package including a plurality of first conductive traces formed on the surface of the encapsulation body. This teaching can be seen in Fig. 4h, where the conductive traces (72) are disposed on the surface of the encapsulation body. Although a dielectric layer (81) lies between the conductive traces and the encapsulation body, the word "on" has not been taken to imply direct contact, and does not require direct contact.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWO



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